TRA-QSFP-100G-ZR4

100G-1310nm / 80km / Gigabit Ethernet 10GBASE-ZR4

PRODUCT FEATURES

- QSFP28 MSA compliant
- Hot pluggable 38 pin electrical interface
- 4 LAN-WDM lanes MUX/DEMUX design
- 4x25G electrical interface
- Maximum power consumption 5.5W
- LC duplex connector
- Supports 103.125Gb/s aggregate bit rate
- Up to 80km transmission on single mode fiber
- Operating case temperature: 0℃ to 70℃
- Single 3.3V power supply
- RoHS 2.0 compliant

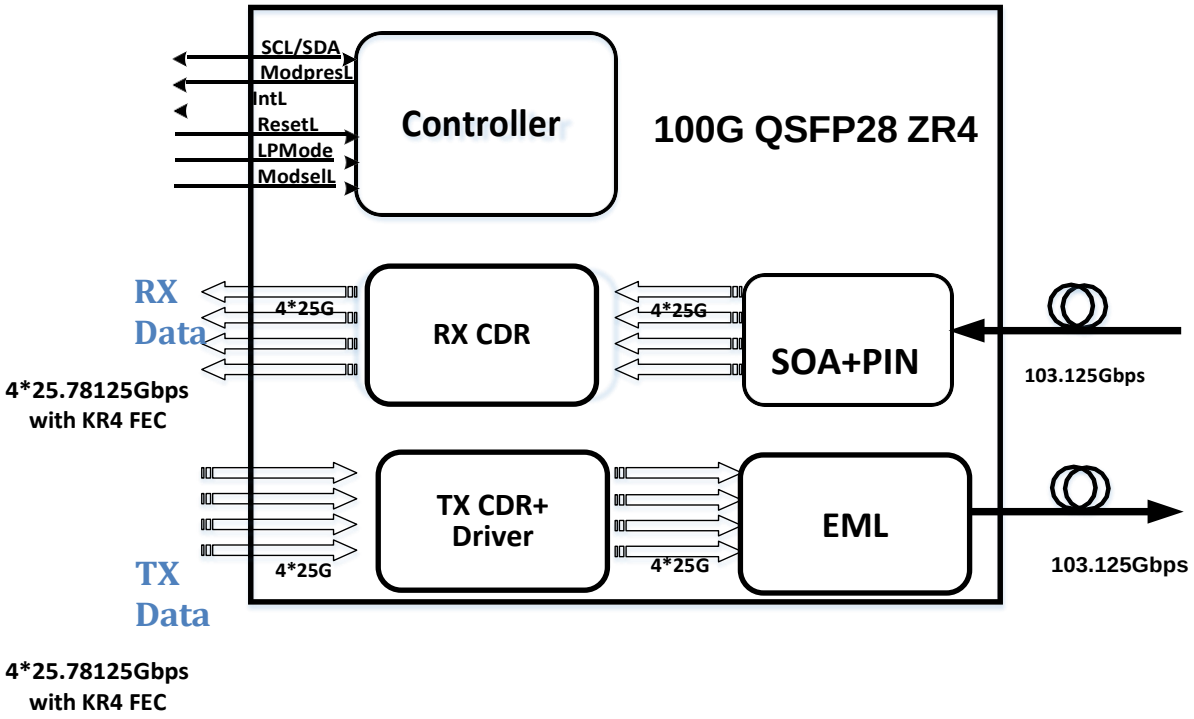
APPLICATIONS

- 100GBASE-ZR4 100G Ethernet
- Telecom networking

DESCRIPTIONS

TRansceiver Asia is designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wire serial inter- face. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. A block diagram is shown in Figure 1.

Transceiver Block Diagrams



ModSelL:

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of theModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL :

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the

Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode:

The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2).

ModPrsL:

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL:

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pinis an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deas-serted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

Pin Descriptions

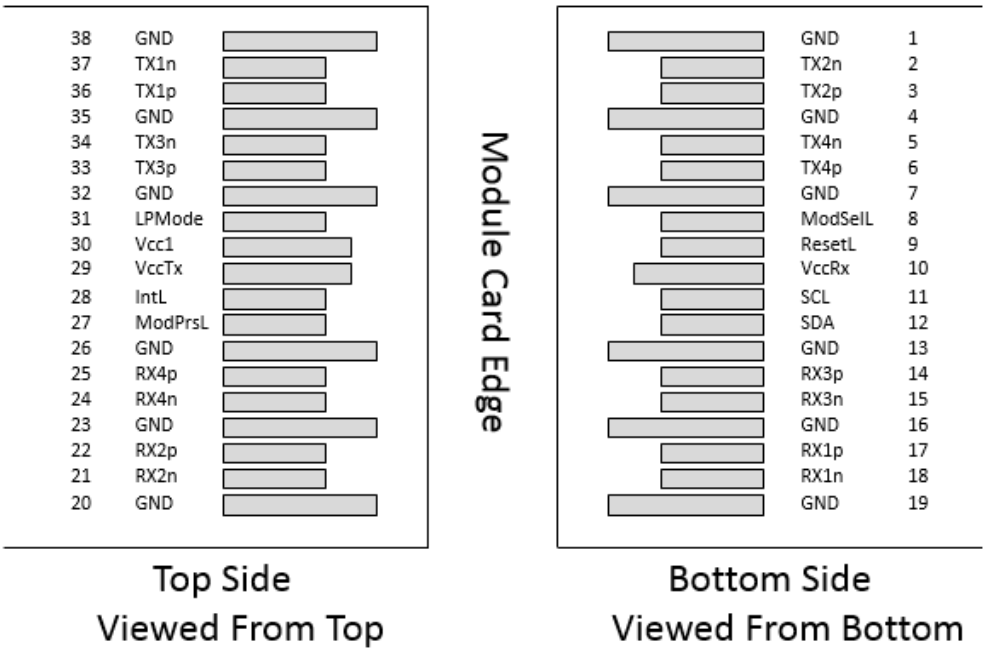


Figure 2. MSA compliant Connector

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes

1.Circuit ground is internally isolated from chassis ground.

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	0		3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	5		85	%	1
Damage Threshold, each lane	THd	6.5			dBm	

Notes

1. Non-condensing

Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.135	3.3	3.465	V
Case Temperature	Top	0		70	℃
Link Distance with G.652				80	km

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power dissipation				5.5	W	
Supply Current	Icc			1.5873	A	Steady state
Transmitter						
Data Rate, each lane			25.78125		Gbps	
Differential Voltage pk-pk	Vpp			900	mV	At 1 MHz
Common Mode Voltage	Vcm	-350		2850	mV	
Transition time	Trise/Tfall	10			ps	20%~80%

Differential Termination Resistance Mismatch				10	%	
Eye width	EW15	0.46			UI	
Eye height	EH15	95			mV	
Receiver						
Data Rate, each lane			25.78125		Gbps	
Differential Termination Resistance Mismatch				10	%	At 1 MHz
Differential output voltage swing	Vout, pp			900	mV	
Common Mode Noise, RMS	Vrms			17.5	mV	
Transition time	Trise/Tfall	12			ps	20%~80%
Eye width	EW15	0.57			UI	
Eye height	EH15	228			mV	

Optical Characteristics

100GBASE-ZR4 Operation（EOL, TOP = 0 to +70 ℃ , VCC = 3.135 to 3.465 Volts）

Parameters	**Unit**	**min**	**type**	**max**	**Note**
Transmitter					
Signaling Speed per Lane	Gb/s	25.78125 ± 100 ppm			
Transmit wavelengths	nm	1294.53		1296.59	
		1299.02		1301.09	
		1303.54		1305.63	
		1308.09		1310.19	
Side-Mode Suppression Ratio (SMSR)	dB	30			
Total Average Launch Power	dBm	8.0		12.5	
Average launch power, each lane	dBm	2.0		6.5	
Difference in launch power between any two lanes (Average and OMA)	dBm			3	
Average launch power of OFF transmitter, each lane	dBm			-30	
Extinction Ratio (ER)	dB	6			

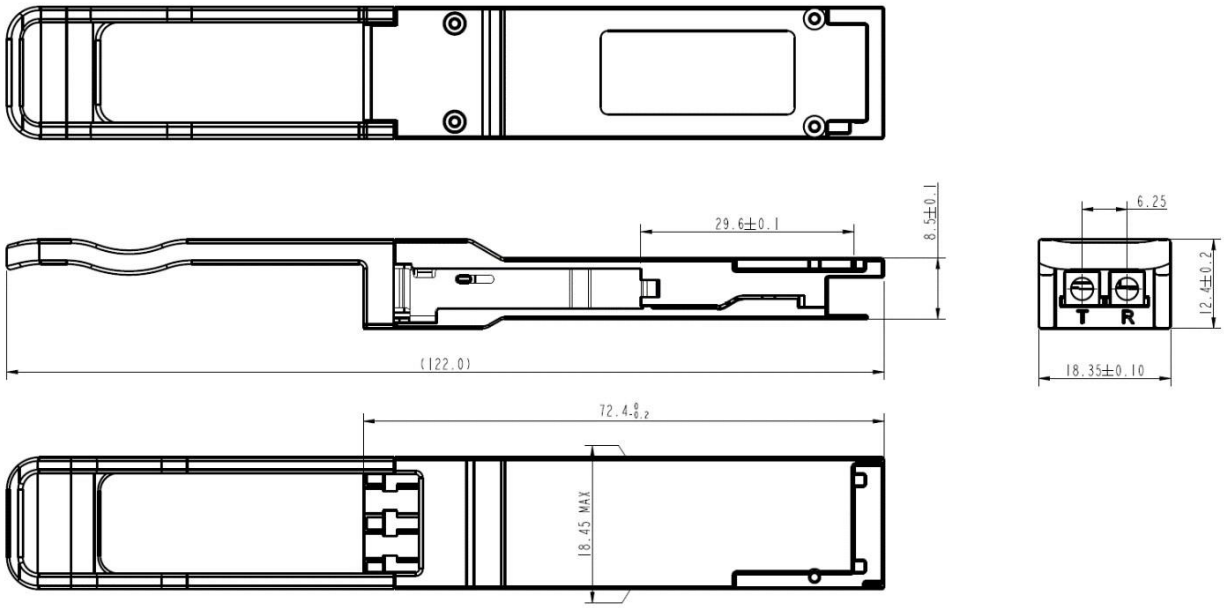
RIN OMA	dB/Hz			-130	
Optical return loss tolerance	dB			20	
Transmitter reflectance	dB			-12	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			1
Mask margin	%	5			
Receiver					
Signaling Speed per Lane	Gb/s	25.78125 ± 100 ppm			
Receive wavelengths	nm	1294.53		1296.59	
		1299.02		1301.09	
		1303.54		1305.63	
		1308.09		1310.19	
Average receiver power, each lane	dBm	-28		-7	
Receiver power, each lane(OMA)	dBm			-7	
Receiver reflectance	dB			-26	
Receiver sensitivity Average, each lane	dBm			-28	1
Receiver 3 dB electrical upper cutoff frequency, each lane	GHz			31	
Damage threshold, each lane	dBm	6.5			
LOS Assert	dBm	-40			
LOS Dessert	dBm			-29	
LOS Hysteresis	dB	0.5			

Notes

1，Sensitivity is specified at BER@5E-5 with FEC

Mechanical Specifications

TRansceiver Asia's TRA-QSFP-100G-ZR4 100G ZR4 QSFP28 transceivers are compatible with the QSFP28 Specificationfor pluggable form factor modules.



Ordering information

Part Number	Description
TRA-SFP-100G-ZR4	QSFP28 ZR4, 1310nm LAN-WDM,Tx(EML),Rx(PIN+SOA),maximum distance 80km on SMF,100 Gigabit Ethernet, dual LC connector, pull-tab, 5.5W, 0°C to 70°C, DDM

Warnings

Process plug

The transceiver optics is supplied with a dust cover. This plug protects the transceiver optics during standard manufacturing processes by preventing contamination from air borne particles. It is recommended that the dust cover remain in the transceiver whenever an optical fiber connector is not inserted.

Handling Precautions

The transceiver optics is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety

The transceiver optics is a Class 1 laser product per international standard IEC 60825-1. Radiation emitted by laser